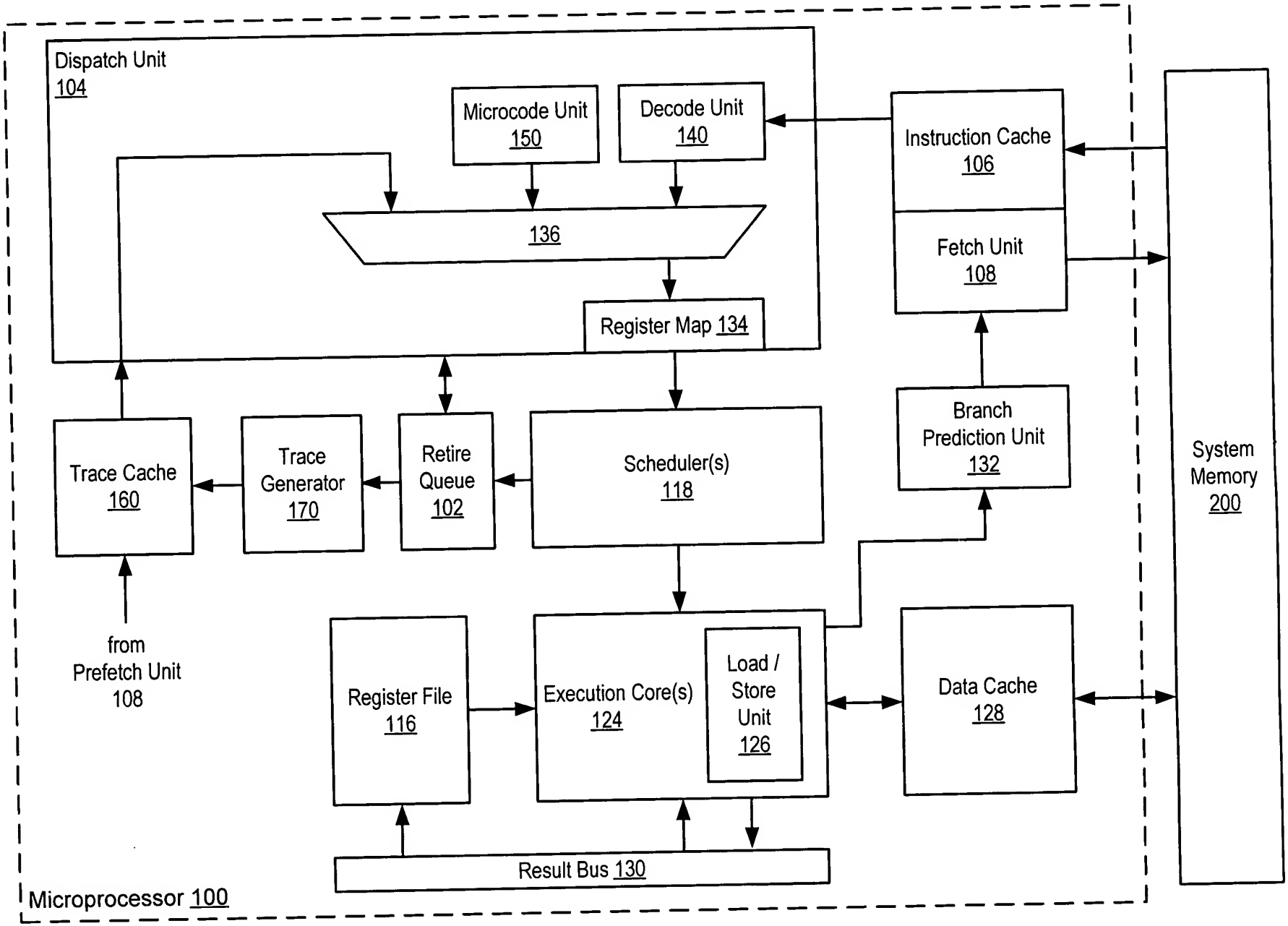
Dispatch Unit
104
Microcode Unit
150
Decode Unit
140
136
Register Map 134
Instruction Cache
106
Fetch Unit
108
Branch
Prediction Unit
132
System
Memory
200
Trace Cache
160
Trace
Generator
170
Retire
Queue
102
Scheduler(s)
118
from
Prefetch Unit
108
Register File
116
Execution Core(s)
124
Load /
Store
Unit
126
Data Cache
128
Result Bus 130
Microprocessor 100

FIG. 1

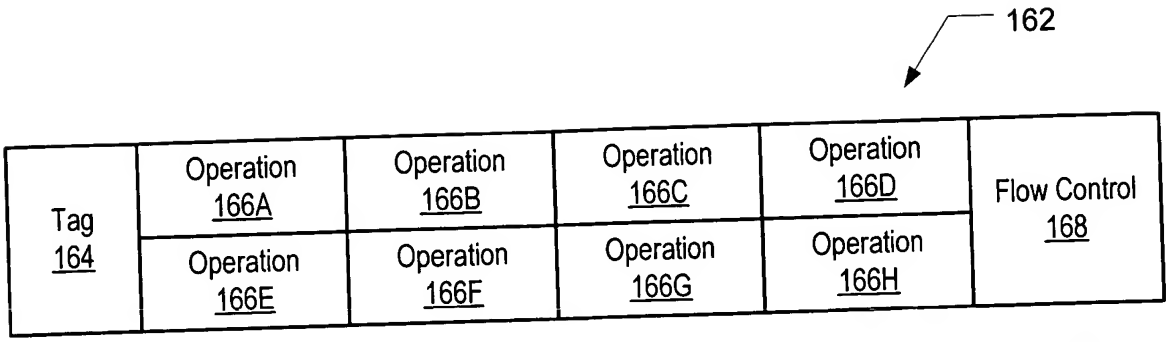

FIG. 2A

Liveness	Encoding 266
Unconditionally Live	11
Subsequent to 1st Branch	10
Subsequent to 2nd Branch	01
Unconditionally Dead	00

FIG. 2B

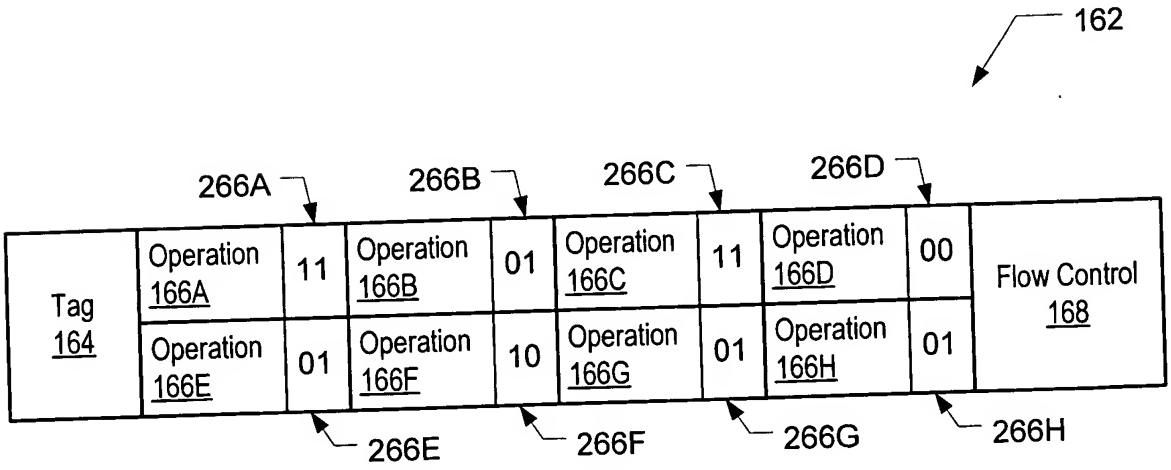

FIG. 2C

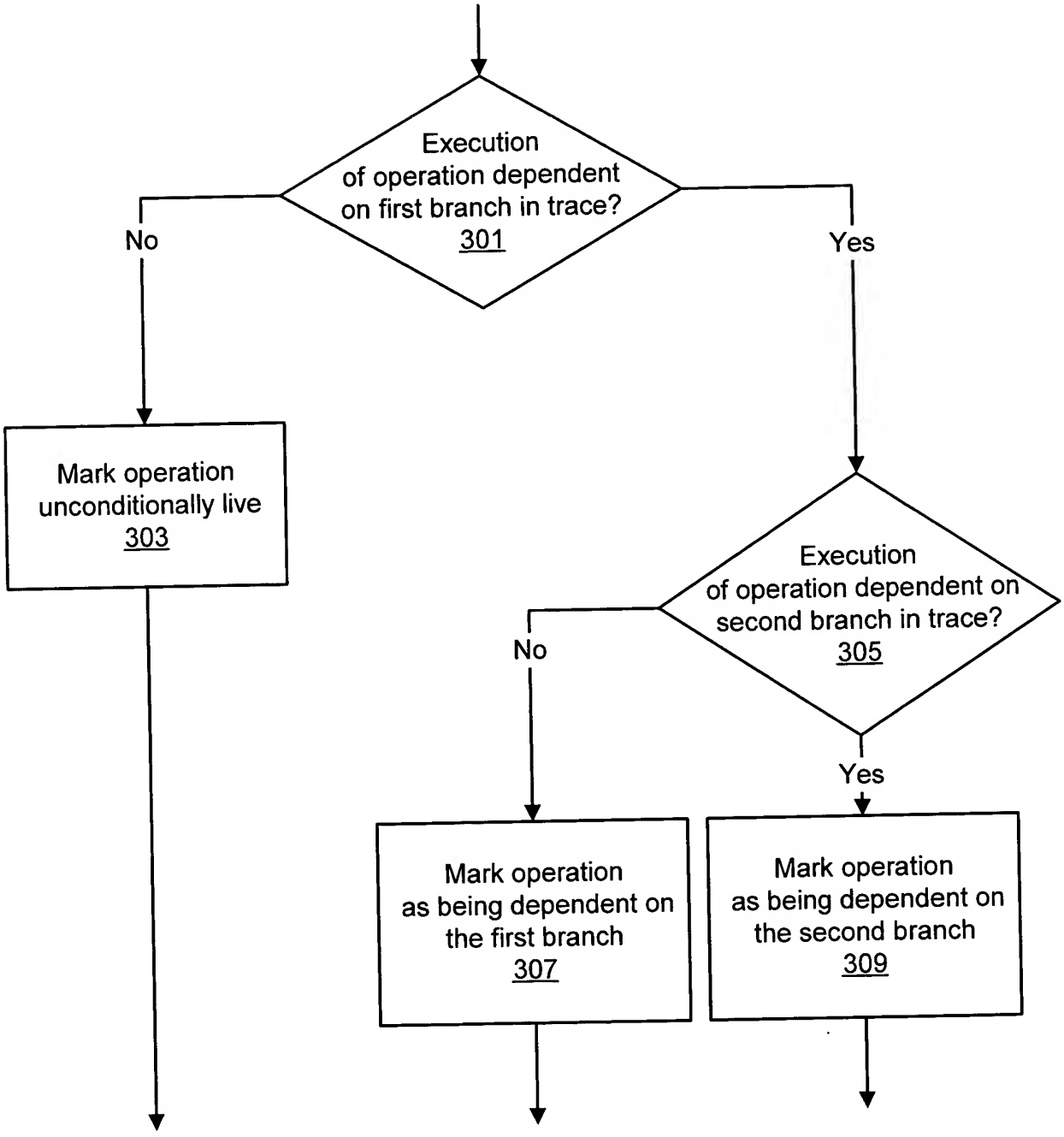
Execution of operation dependent on first branch in trace? 301
No
Yes
Mark operation unconditionally live 303
Execution of operation dependent on second branch in trace? 305
No
Yes
Mark operation as being dependent on the first branch 307
Mark operation as being dependent on the second branch 309

FIG. 3

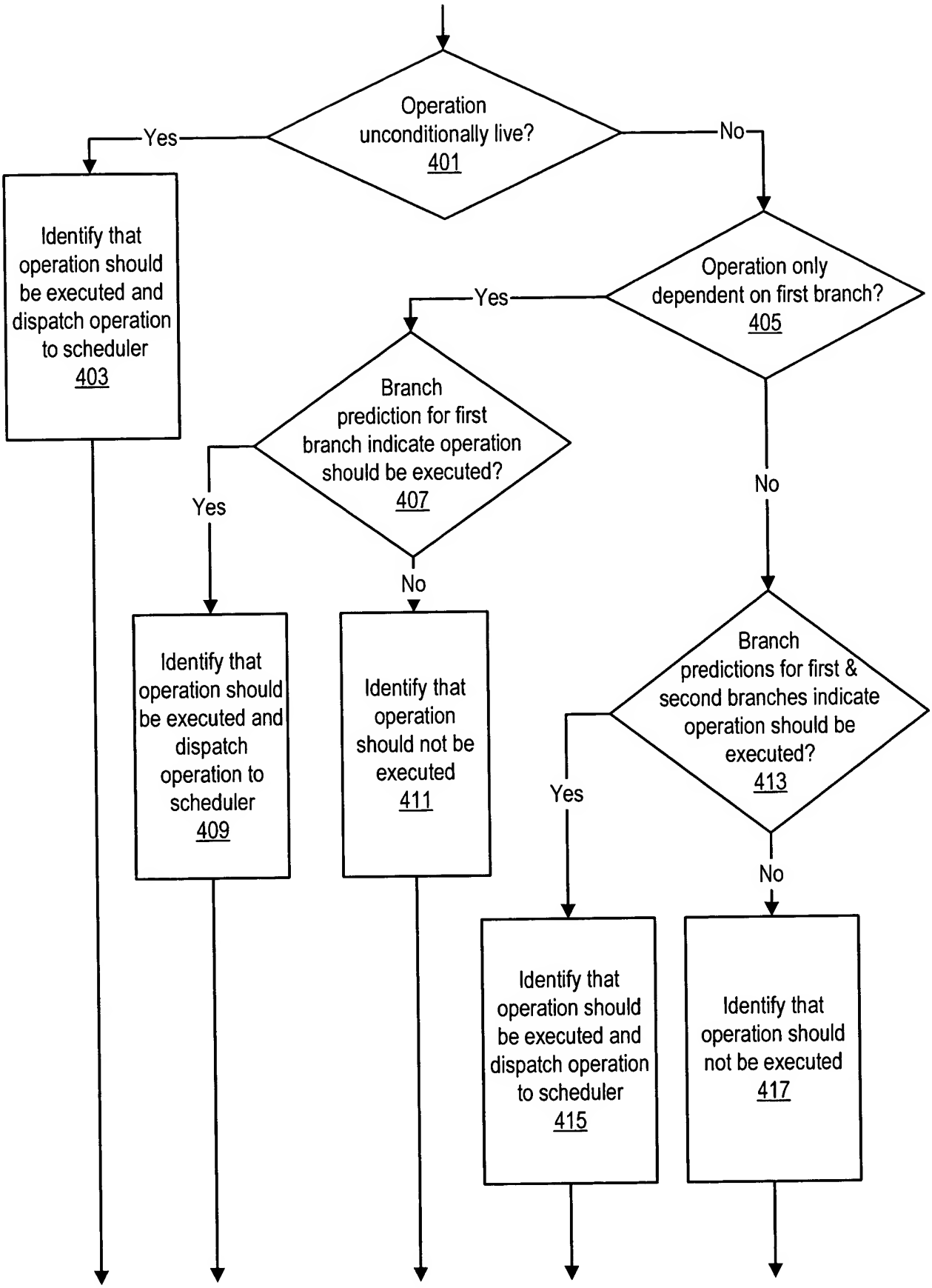
Operation unconditionally live? 401
Yes
No
Identify that operation should be executed and dispatch operation to scheduler 403
Operation only dependent on first branch? 405
Yes
No
Branch prediction for first branch indicate operation should be executed? 407
Yes
No
Identify that operation should be executed and dispatch operation to scheduler 409
Identify that operation should not be executed 411
Branch predictions for first & second branches indicate operation should be executed? 413
Yes
No
Identify that operation should be executed and dispatch operation to scheduler 415
Identify that operation should not be executed 417

FIG. 4

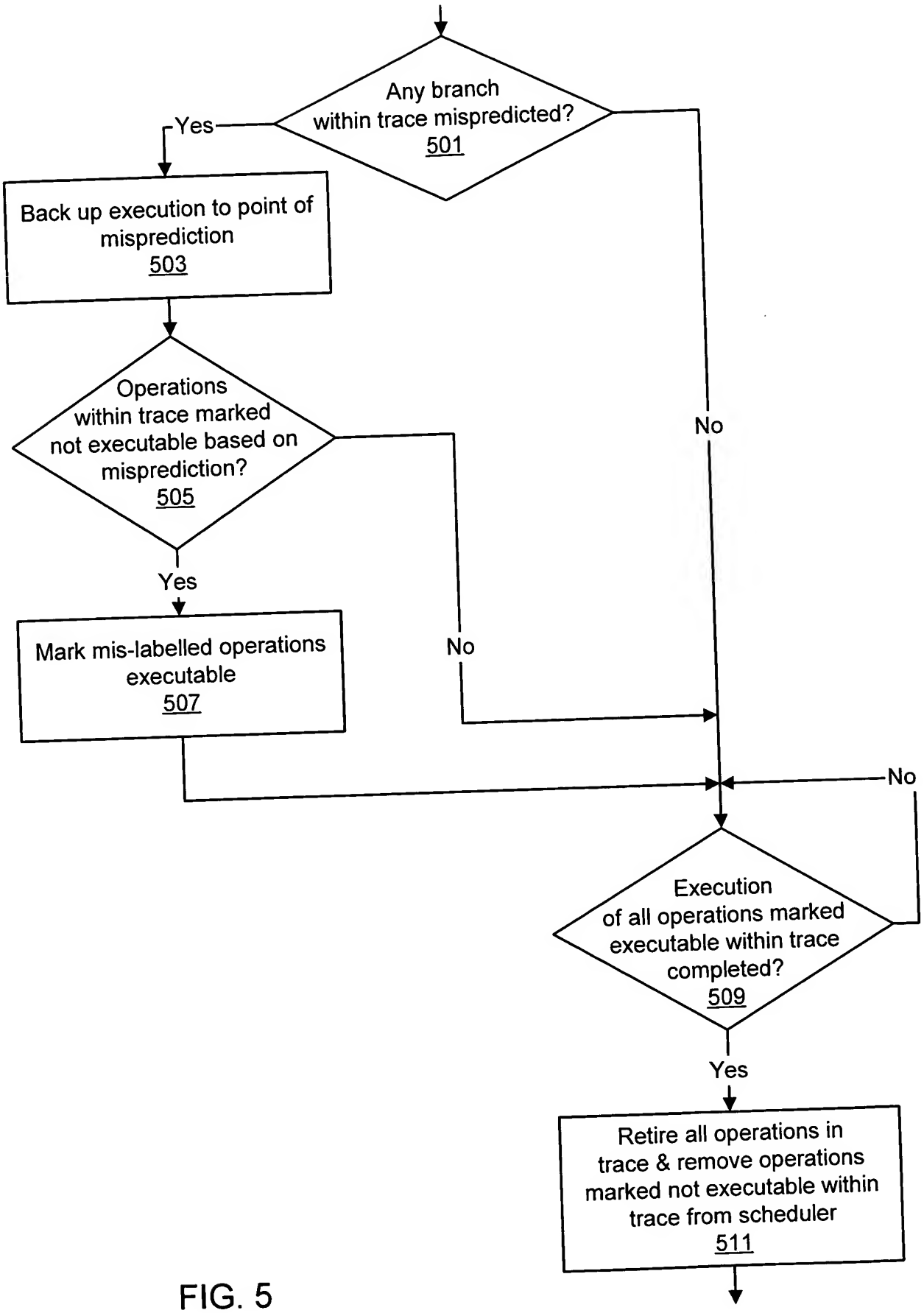
Any branch within trace mispredicted? 501
Yes
No
Back up execution to point of misprediction 503
Operations within trace marked not executable based on misprediction? 505
Yes
No
Mark mis-labelled operations executable 507
No
Execution of all operations marked executable within trace completed? 509
Yes
Retire all operations in trace & remove operations marked not executable within trace from scheduler 511

FIG. 5

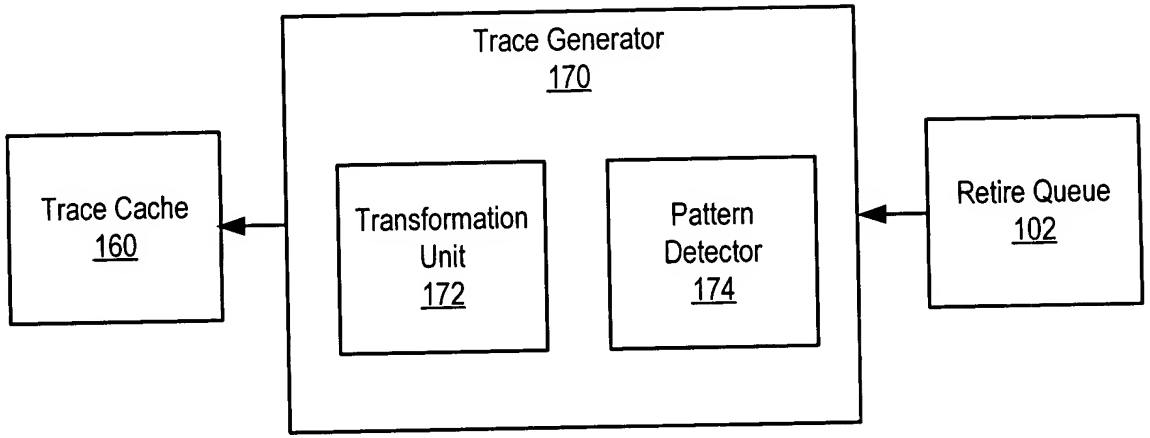
Trace Generator
170
Trace Cache
160
Transformation
Unit
172
Pattern
Detector
174
Retire Queue
102

FIG. 6

Before Constant Propagation:

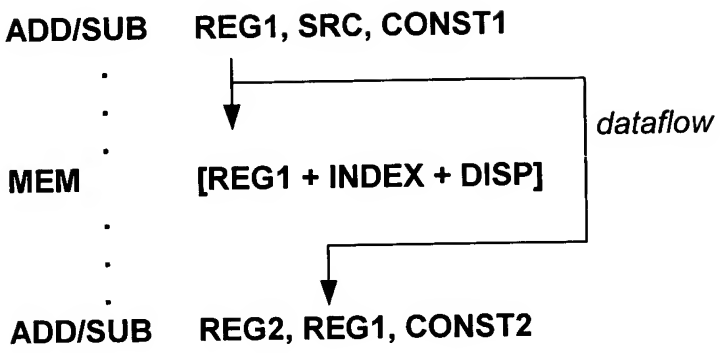

FIG. 7A

After Constant Propagation:

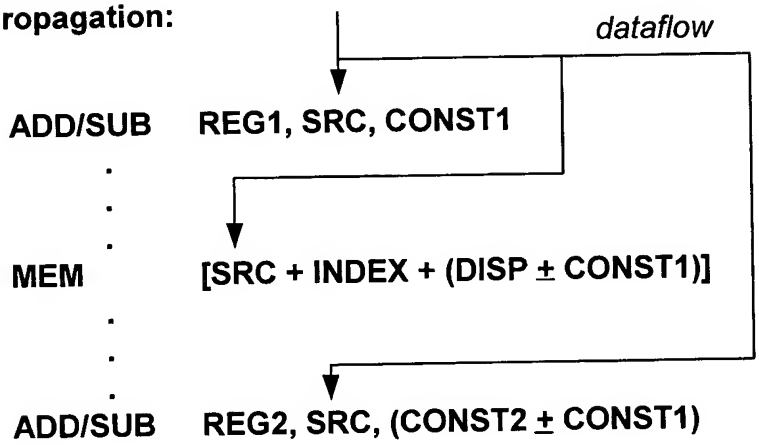

FIG. 7B

Before Mov Renaming:

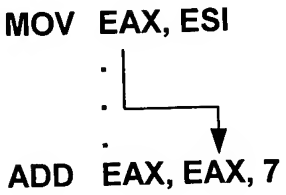

FIG. 8A

After Move Renaming:

ADD EAX, ESI, 7

FIG. 8B

Before Move Renaming:

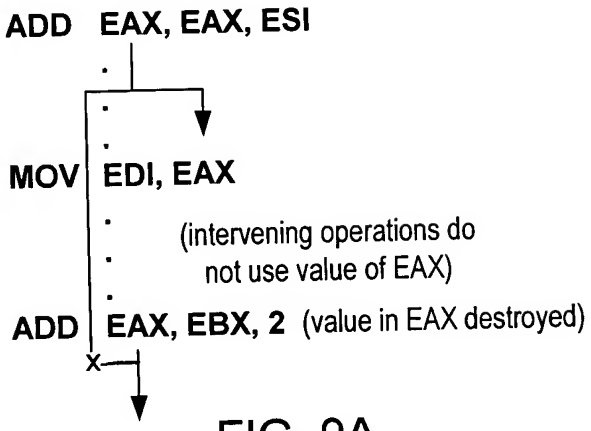

FIG. 9A

After Move Renaming:

ADD EDI, EAX, ESI

ADD EAX, EBX, 2

FIG. 9B

Before any transformations:

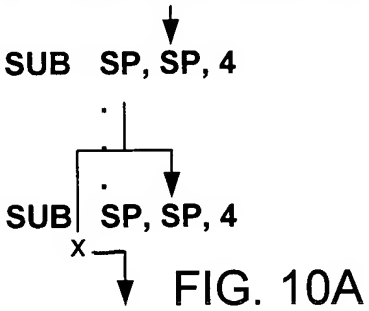

FIG. 10A

Slotification:

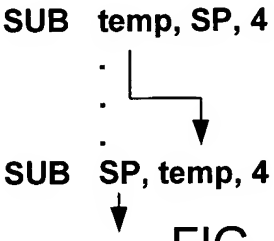

FIG. 10B

After Constant Propagation:

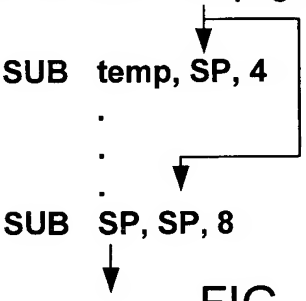

FIG. 10C

After Dead Operation Elimination:

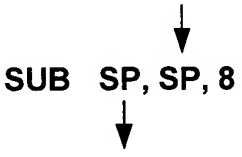

FIG. 10D

Befor :

Op1 Sets condition code

- (intervening instructions do
- not set condition code)
-

JNE Label

FIG. 11A

After Branch Folding:

Op1 Sets condition code; fail if NE

FIG. 11B

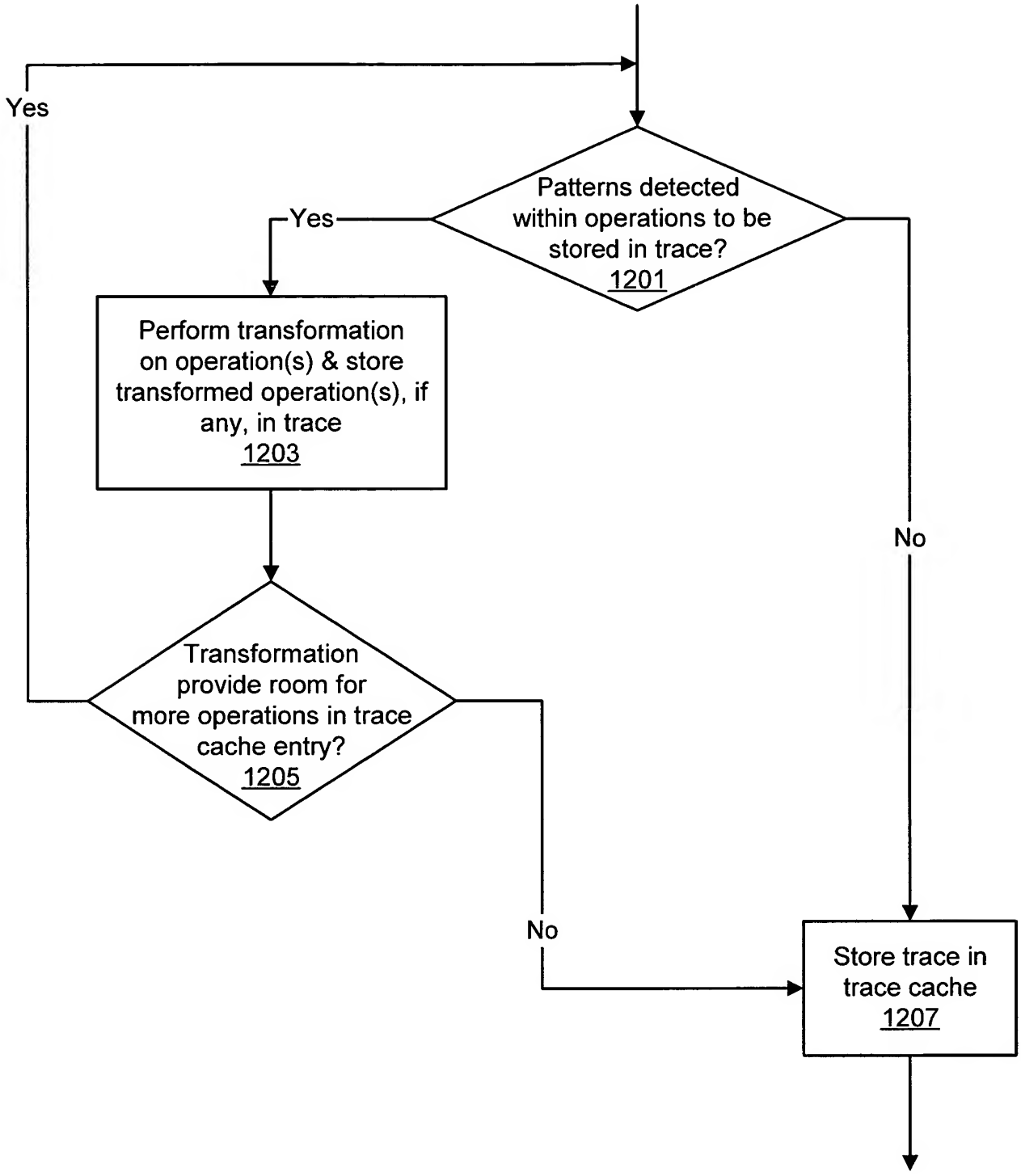
Yes
Patterns detected within operations to be stored in trace?
1201
Yes
Perform transformation on operation(s) & store transformed operation(s), if any, in trace
1203
No
Transformation provide room for more operations in trace cache entry?
1205
No
Store trace in trace cache
1207

FIG. 12

Instruction Stream:

Instruction1
Instruction2
Instruction3
Microcoded Instruction
Instruction4
Instruction5
.
.
.

FIG. 13A

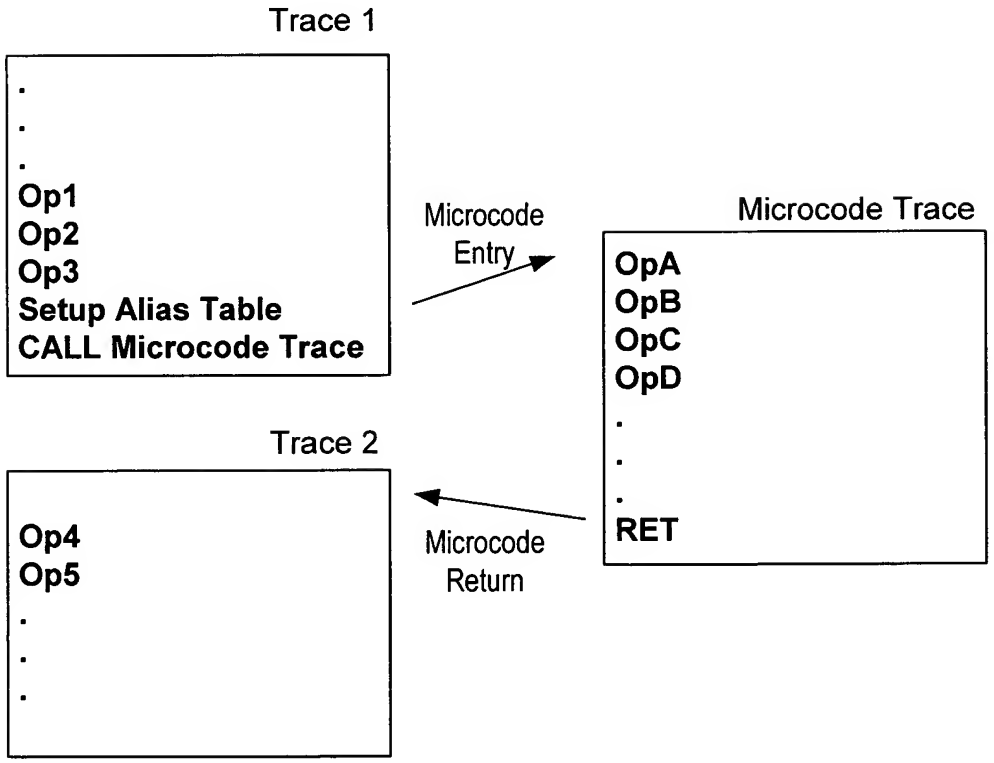

FIG. 13B

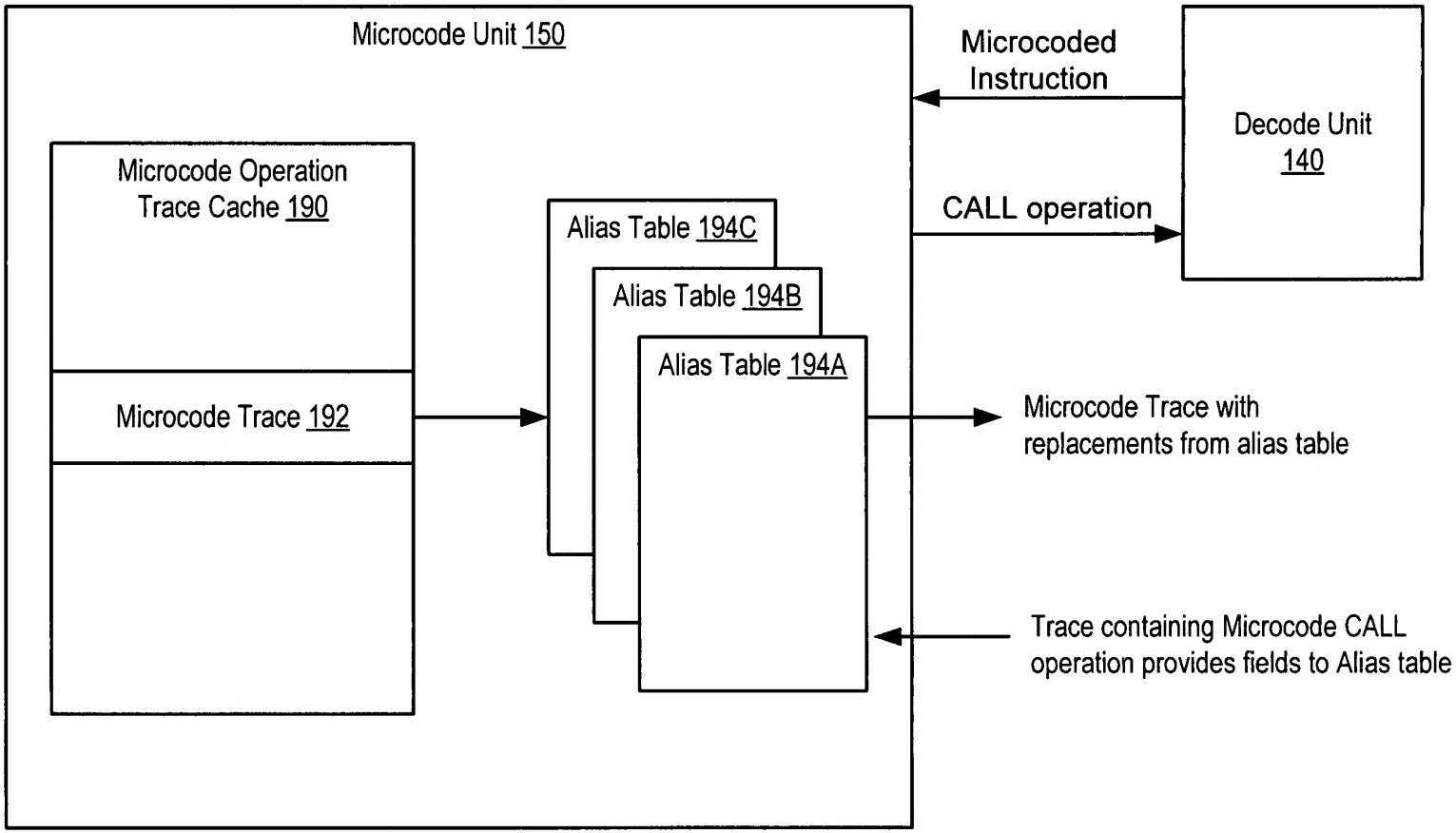
Microcode Unit 150
Microcoded Instruction
Decode Unit 140
Microcode Operation Trace Cache 190
CALL operation
Alias Table 194C
Alias Table 194B
Alias Table 194A
Microcode Trace 192
Microcode Trace with replacements from alias table
Trace containing Microcode CALL operation provides fields to Alias table

FIG. 13C

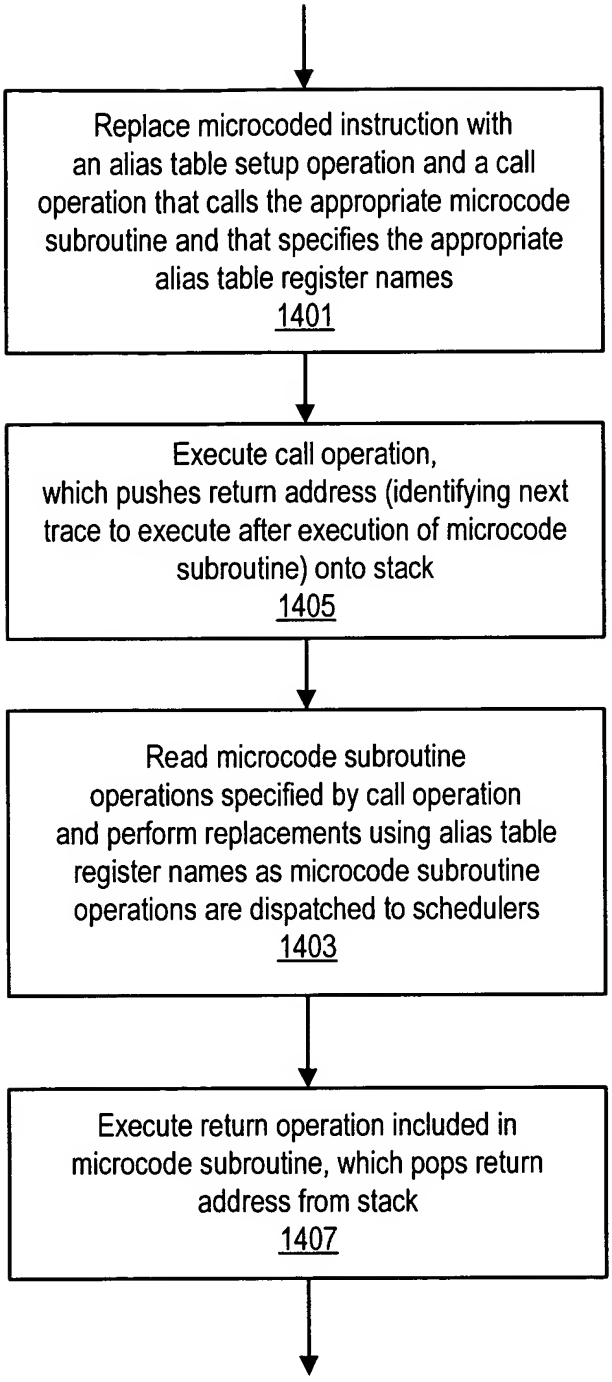
Replace microcoded instruction with an alias table setup operation and a call operation that calls the appropriate microcode subroutine and that specifies the appropriate alias table register names
1401
Execute call operation, which pushes return address (identifying next trace to execute after execution of microcode subroutine) onto stack
1405
Read microcode subroutine operations specified by call operation and perform replacements using alias table register names as microcode subroutine operations are dispatched to schedulers
1403
Execute return operation included in microcode subroutine, which pops return address from stack
1407

FIG. 14

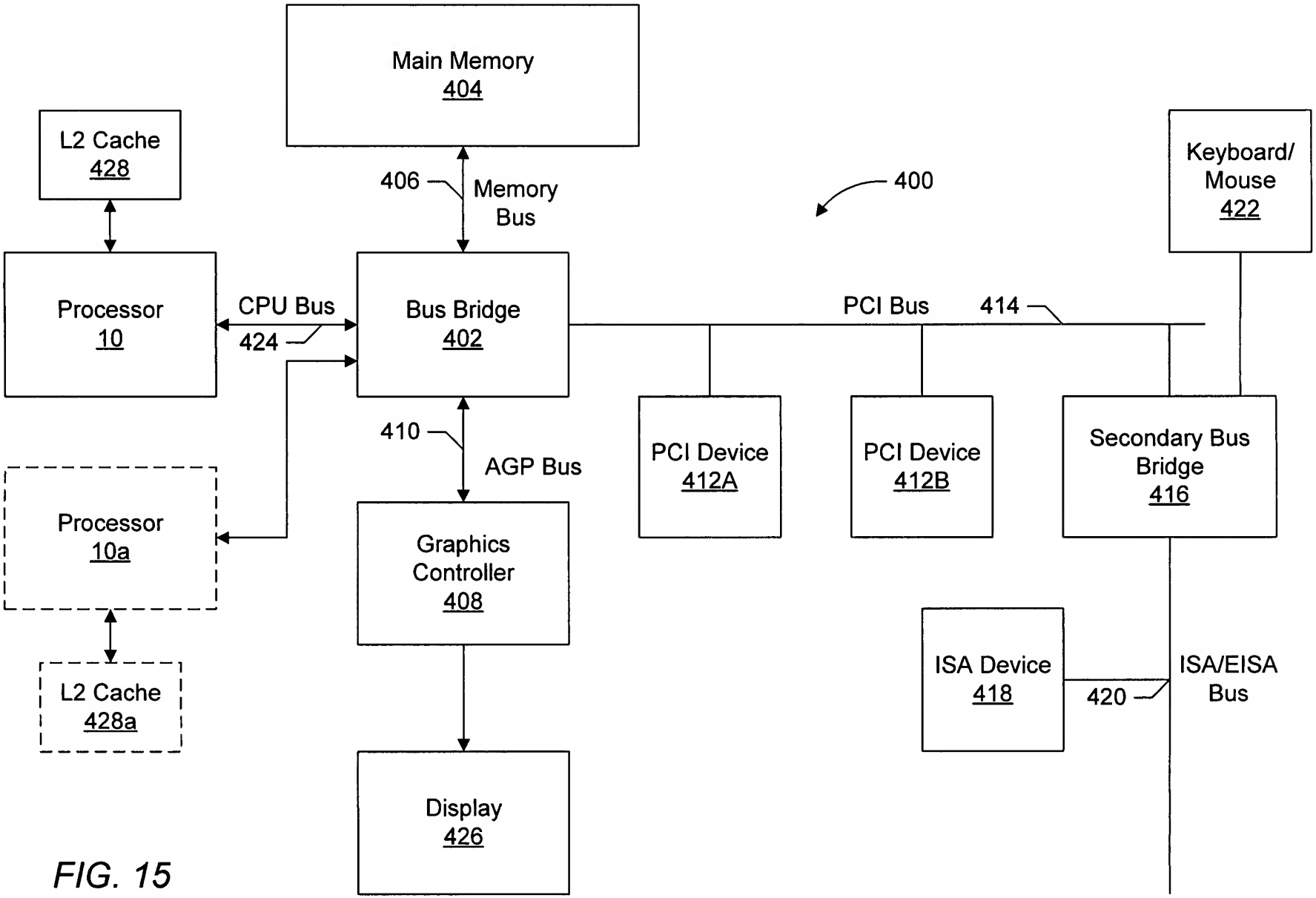
Main Memory
404
L2 Cache
428
406
Memory
Bus
400
Keyboard/
Mouse
422
Processor
10
CPU Bus
424
Bus Bridge
402
PCI Bus
414
410
AGP Bus
PCI Device
412A
PCI Device
412B
Secondary Bus
Bridge
416
Processor
10a
Graphics
Controller
408
ISA Device
418
420
ISA/EISA
Bus
L2 Cache
428a
Display
426

FIG. 15

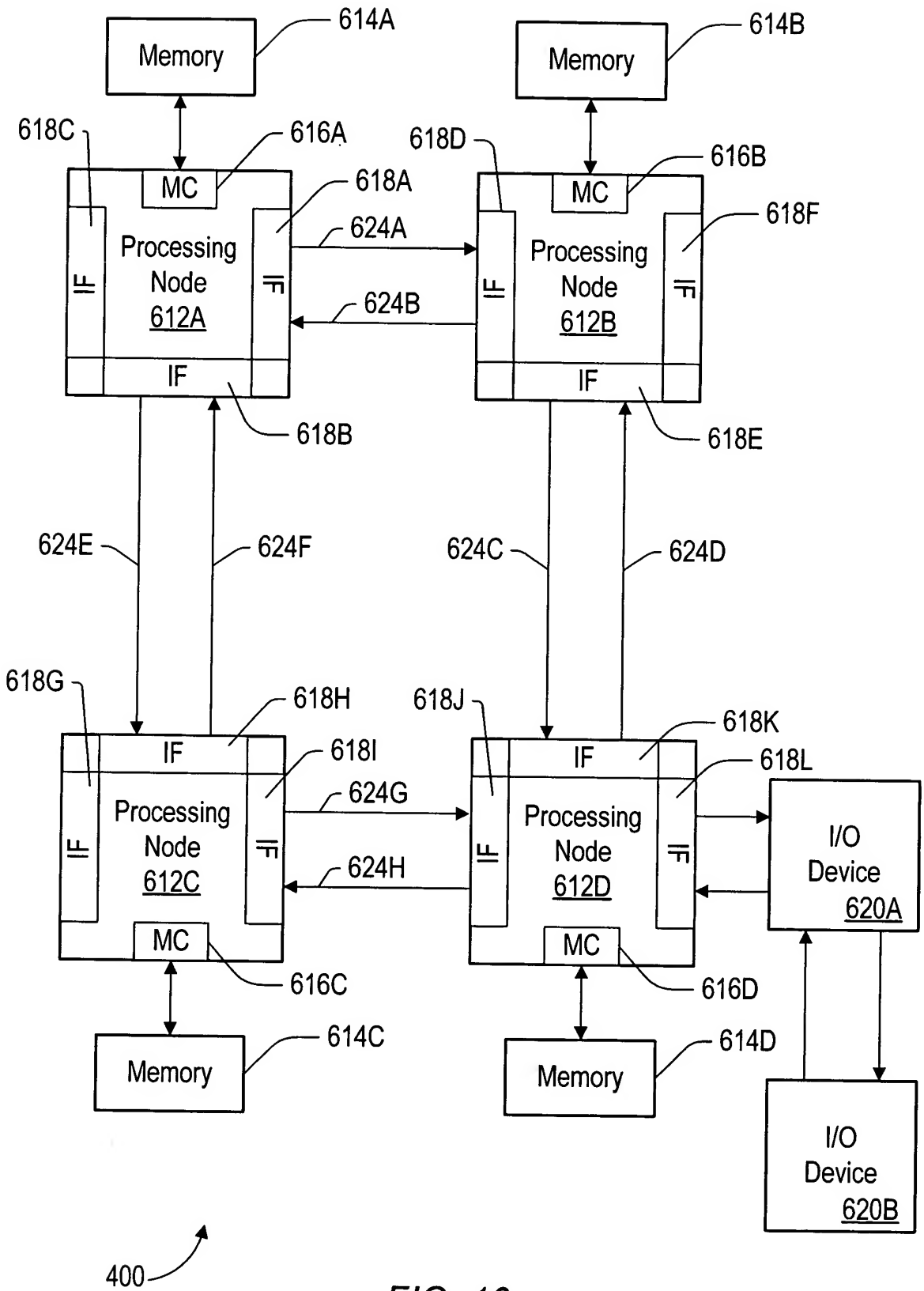
Memory
614A
Memory
614B
618C
616A
618D
616B
MC
MC
618A
618F
624A
Processing Node 612A
Processing Node 612B
624B
IF
IF
IF
IF
IF
IF
618B
618E
624E
624F
624C
624D
618G
618H
618J
618K
IF
IF
618I
618L
624G
Processing Node 612C
Processing Node 612D
I/O Device 620A
624H
MC
MC
616C
616D
Memory
614C
Memory
614D
I/O Device 620B
400

FIG. 16